R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

OBJECTION TO THE SPECIFICATION

The objection to the specification under 35 U.S.C. §112, first paragraph, for failing to comply with the written description requirement to support the subject matter set forth in the claims is respectfully traversed and should be withdrawn.

The conclusory statement that "the specification, as originally filed does not provide support for the invention now claimed" does not adequately meet the Patent Office's burden to factually establish a *prima facie* showing under 35 U.S.C. §112, first paragraph.

The Office has previously admitted that the specification describes the delay times as providing "any appropriate delay in order to meet the criteria of a particular implementation" (see page 3, lines 13-15 of the Office Action dated March 1, 2004 (paper no. 10) citing page 7, lines 10-11 of the specification). Clearly "any appropriate delay" would be understood by one of ordinary skill in the field of the invention as broad enough to include delays that can be described as less than a period of the clock signal. The specification further states:

> For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay

> of the signal DLY appropriate with a circuit such as the circuit 20 of FIG. 2 (page 9,line 17 through page 10, line 1 of the specification).

The specification recites that the circuit 10 requires an aggressive data setup time and the circuit 20 requires an aggressive data hold time (see page 1, line 15 through page 2, line 10 of the specification. Thus, the specification clearly provides that the delay elements 109a-109n can provide delays on the order of an aggressive setup time and an aggressive hold time.

One skilled in the art would clearly be aware of the definitions of the terms "setup time" and "hold time," as evidenced by Fletcher, William I., An Engineering Approach to Digital Design, Prentice-Hall Inc., 1980, pages 320-323 (hereinafter Fletcher; which was previously submitted and is attached as Exhibit A). In particular, one of ordinary skill in the art would understand that the setup time is the time required for the input data to settle in before the triggering edge of the clock signal (see definition of set-up time in section 5-20 on page 323 of Fletcher). Furthermore, one of ordinary skill in the art would understand that the definition of hold time is the time required for the data to remain stable after the triggering edge of the clock signal (see definition of hold time in section 5-20 on page 323 of Fletcher). These definitions are consistent with the use of the terms in the specification (see page 1, lines 10-14 of the specification.

Furthermore, one of ordinary skill in the art would understand that the setup time and the hold time involve delay

times that are less than the period of the clock signal (see FIGS. 5-38 and 5-41 in Fletcher). Furthermore, one of ordinary skill in the art would understand that a setup time or hold time greater than a period of the clock signal would not be reasonable since setup and hold time are defined with respect to a transition of the clock signal immediately following the setup time and immediately preceding the hold time.

FIG. 5, as originally filed, illustrates a circuit 100 comprising a plurality of delay devices 109a-109n connected in series. The specification states:

> Referring to FIG. 5, a detailed block diagram of the circuit 100 is shown. The circuit 100 of FIG. 5 illustrates an overall detailed implementation of the present invention. The circuit 101 may comprise the HSTL block 108, the delay devices 109a-109n and the multiplexer 111. The register 102 may be implemented, in one example, as a "D" type register. However, the register 102 may be implemented as another appropriate type register in order to meet the criteria of a particular implementation.
>
> **The circuit 100 may provide optimal setup and hold timing solutions.** The circuit 100 may provide a configurable delay for (i) data and/or (ii) clock signals. The circuit 100 may overcome performance degradation associated with a single timing setup. **The circuit 100 may provide reduced performance degradation of data setup and/or hold times.** Additionally, the circuit 100 may provide a user configurable delay (page 8, line 14 through page 9, line 9 of the specification as originally filed, emphasis added).

Furthermore, one of ordinary skill in the art would recognize that since the delay devices are connected in series, a delay time provided by the circuit 100 is determined by the number of the

delay devices through which a signal passes before being presented at the output of the switch 111.

Because (a) setup time and hold time are defined with respect to a triggering edge of the clock signal and would be understood by one of ordinary skill in the art to be less than a period of the clock signal and (b) the delay time provided by the circuit 100 as illustrated in FIG. 5 (i) is determined by the sum of the individual delay times of the delay devices 109a-109n through which a signal passes and (ii) may provide optimal setup and hold timing, one of ordinary skill in the art would recognize FIG. 5 and the related description in the specification, as originally filed, as supporting the limitation that "a total of all of said plurality of delay times is less than the period of the clock signal," as presently claimed. Therefore, the disclosure of the application as originally filed, reasonably conveys to the artisan that the inventor had possession, at the time the application was filed, of the presently claimed subject matter. *Vas Cath, Inc. v. Mahurkar*, 935 F. 2d. 1555, 1565, 19 USPQ2d. 1111, 1118 (Fed. Cir. 1991), *reh'rg denied* (Fed. Cir. July 8, 1991) and *reh'rg, en banc, denied* (Fed. Cir. July 29, 1991). As such, the specification complies with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

Furthermore, a patent need not teach, and preferably omits, what is well known in the art (MPEP §2164.01). The art of record may provide evidence of the level of knowledge of one of

ordinary skill in the relevant art. The Office Action asserts that the art of record (i.e. Table 2 of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999) shows each of the plurality of delay times is less than a period of the clock signal. Thus, one of ordinary skill in the art would know of delay times that are less than a clock period. Therefore, the disclosures in the specification in the light of information known in the art would reasonably convey to the skilled artisan that the inventor had possession at the time of the invention of the claimed subject matter. As such, the specification complies with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The rejection of claim 21 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one of skill in the relevant art that the inventor, at the time of the application was filed, had possession of the claimed invention is respectfully traversed and should be withdrawn.

The Office Action fails to present any objective evidence or convincing line of reasoning to support the conclusory statement that the limitation "wherein a total of all said plurality of delay times is less that [sic: than] said period of said clock" is not described by the specification in such a way as to reasonably convey to one of skill in the relevant art that the inventor, at

the time of the application was filed, had possession of the claimed invention. As such, the rejection does not appear to be proper and should be withdrawn.

Furthermore, the Office has previously admitted that the specification describes the delay times as providing "any appropriate delay in order to meet the criteria of a particular implementation" (see page 3, lines 13-15 of the Office Action dated March 1, 2004 (paper no. 10) citing page 7, lines 10-11 of the specification). Clearly "any appropriate delay" would be understood by one of ordinary skill in the field of the invention as broad enough to include delays that can be described as less than a period of the clock signal. The specification further states:

> For example, one of the delay elements 109a-109n may be appropriate to provide timing that may be used with a circuit such as the circuit 10 of FIG. 1. Furthermore, another one of the delay elements 109a-109n may provide a delay of the signal DLY appropriate with a circuit such as the circuit 20 of FIG. 2 (page 9,line 17 through page 10, line 1 of the specification).

The specification recites that the circuit 10 requires an aggressive data setup time and the circuit 20 requires an aggressive data hold time (see page 1, line 15 through page 2, line 10 of the specification. Thus, the specification clearly provides that the delay elements 109a-109n can provide delays on the order of an aggressive setup time and an aggressive hold time.

One skilled in the art would clearly be aware of the definitions of the terms "setup time" and "hold time," as evidenced

by Fletcher, William I., An Engineering Approach to Digital Design, Prentice-Hall Inc., 1980, pages 320-323 (hereinafter Fletcher; which was previously submitted and is attached as Exhibit A). In particular, one of ordinary skill in the art would understand that the setup time is the time required for the input data to settle in before the triggering edge of the clock signal (see definition of set-up time in section 5-20 on page 323 of Fletcher). Furthermore, one of ordinary skill in the art would understand that the definition of hold time is the time required for the data to remain stable after the triggering edge of the clock signal (see definition of hold time in section 5-20 on page 323 of Fletcher). These definitions are consistent with the use of the terms in the specification (see page 1, lines 10-14 of the specification.

Furthermore, one of ordinary skill in the art would understand that the setup time and the hold time involve delay times that are less than the period of the clock signal (see FIGS. 5-38 and 5-41 in Fletcher). Furthermore, one of ordinary skill in the art would understand that a setup time or hold time greater than a period of the clock signal would not be reasonable since setup and hold time are defined with respect to a transition of the clock signal immediately following the setup time and immediately preceding the hold time.

FIG. 5, as originally filed, illustrates a circuit 100 comprising a plurality of delay devices 109a-109n connected in series. The specification states:

> Referring to FIG. 5, a detailed block

> diagram of the circuit 100 is shown. The circuit 100 of FIG. 5 illustrates an overall detailed implementation of the present invention. The circuit 101 may comprise the HSTL block 108, the delay devices 109a-109n and the multiplexer 111. The register 102 may be implemented, in one example, as a "D" type register. However, the register 102 may be implemented as another appropriate type register in order to meet the criteria of a particular implementation.
>
> **The circuit 100 may provide optimal setup and hold timing solutions.** The circuit 100 may provide a configurable delay for (i) data and/or (ii) clock signals. The circuit 100 may overcome performance degradation associated with a single timing setup. **The circuit 100 may provide reduced performance degradation of data setup and/or hold times.** Additionally, the circuit 100 may provide a user configurable delay (page 8, line 14 through page 9, line 9 of the specification as originally filed, emphasis added).

Furthermore, one of ordinary skill in the art would recognize that since the delay devices are connected in series, a delay time provided by the circuit 100 is determined by the number of the delay devices through which a signal passes before being presented at the output of the switch 111.

Because (a) setup time and hold time are defined with respect to a triggering edge of the clock signal and would be understood by one of ordinary skill in the art to be less than a period of the clock signal and (b) the delay time provided by the circuit 100 as illustrated in FIG. 5 (i) is determined by the sum of the individual delay times of the delay devices 109a-109n through which a signal passes and (ii) may provide optimal setup and hold timing, one of ordinary skill in the art would recognize FIG. 5 and the related description in the specification, as

originally filed, as supporting the limitation that "a total of all of said plurality of delay times is less than the period of the clock signal," as presently claimed. Therefore, the disclosure of the application as originally filed, reasonably conveys to the artisan that the inventor had possession, at the time the application was filed, of the presently claimed subject matter. *Vas Cath, Inc. v. Mahurkar*, 935 F. 2d. 1555, 1565, 19 USPQ2d. 1111, 1118 (Fed. Cir. 1991), *reh'rg denied* (Fed. Cir. July 8, 1991) and *reh'rg, en banc, denied* (Fed. Cir. July 29, 1991). As such, the specification complies with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

Furthermore, a patent need not teach, and preferably omits, what is well known in the art (MPEP §2164.01). The art of record may provide evidence of the level of knowledge of one of ordinary skill in the relevant art. The Office Action asserts that the art of record (i.e. Table 2 of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999) shows each of the plurality of delay times is less than a period of the clock signal. Thus, one of ordinary skill in the art would know of delay times that are less than a clock period. Therefore, the disclosures in the specification in the light of information known in the art would reasonably convey to the skilled artisan that the inventor had possession at the time of the invention of the claimed subject matter. As such, the specification complies

with the written description requirement under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-3, 11-13, 15-21 and 23 under 35 U.S.C. §103(a) as being unpatentable over Conn et al. (U.S. Patent No. 6, 150,863, hereinafter Conn) in view of Dallas Semiconductor Datasheet, "DS1020 Programmable 8-bit Silicon Delay Line," November 17, 1999 (hereinafter Dallas) is respectfully traversed and should be withdrawn.

The rejection of claims 4-10 under 35 U.S.C. §103(a) as being unpatentable over Conn in view of Dallas and in further view of JEDEC Standard No. 8-6, "High Speed Transceiver Logic (HSTL) - A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits," EIA/JESD8-6, August 1995 (hereinafter JEDEC) is respectfully traversed and should be withdrawn.

The rejection of claim 22 under 35 U.S.C. §103(a) as being unpatentable over Conn in view of Dallas and in further view of Olson (U.S. Patent No. 5,247,617) is respectfully traversed and should be withdrawn.

Conn is directed to a user controlled delay circuit for a programmable logic device (Title). Dallas discloses a programmable 8-bit silicon delay line (Title). Conn and Dallas, alone or in combination, do not teach or suggest each and every element of the presently claimed invention. Specifically, assuming *arguendo*, (i) the clock pad 505 of Conn is similar to the presently

claimed first input, (ii) the IO pad 220A of Conn is similar to the presently claimed second input, (iii) the circuit 210A of Conn is similar to the presently claimed first circuit and (iv) the circuit 510A of Conn is similar to the present claimed second circuit, Conn does not teach or suggest a second circuit configured to receive the delayed data signal from the first circuit and the clock signal **from the first input**, as presently claimed in claim 1.

Furthermore, the Office Action fails to present any objective evidence or convincing line of reasoning why one of ordinary skill in the field of the invention would consider (i) the input of the circuit 510A of Conn as being the same as a first input of an apparatus and (ii) the circuit 510A receiving the clock signal from the first input, as presently claimed. In particular, one of ordinary skill in the art would recognize the signal CLK of Conn at the CK input of the circuit 510A of Conn as received from an output of the delay element 530 of Conn rather than from an input of an apparatus, as presently claimed. Therefore, Conn and Dallas do not appear to teach or suggest each and every element of the presently pending claim 1. Claims 11 and 12 include similar limitations. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, the Examiner's conclusory statement that "a motivation for [combining Conn and Dallas] would have been to 'to satisfy the requirements of a particular application" (page 6, lines 10-11 of the Office Action), fails to adequately address the

issue of motivation to combine. The factual question of motivation is material to patentability and cannot be resolved on subject belief and unknown authority. It is improper in determining whether a person of ordinary skill would have been led to a combination of references simply to use that which the inventor taught against its teacher. The Office Action fails to present any objective evidence, specific findings or convincing line of reasoning why the skilled artisan, with no knowledge of the presently claimed invention, would have selected these references for combination in the manner claimed. The recitation of the generic phrase "to satisfy the requirements of a particular application" (see page 6, lines 10-11 of the Office Action) does not specifically identify the principle, known to one of ordinary skill in the art, that would compel the claimed combination. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-10 and 13-23 depend, directly or indirectly, from either claim 1 or claim 12 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

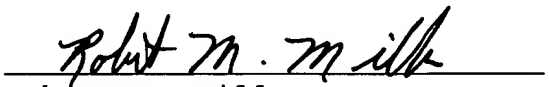
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: November 2, 2004

Docket No.: 0325.00355

Exhibit A
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AN ENGINEERING APPROACH TO DIGITAL DESIGN

WILLIAM I. FLETCHER
Utah State University
Logan, Utah

PRENTICE-HALL, INC., *Englewood Cliffs, New Jersey 07632*

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Library of Congress Cataloging in Publication Data

FLETCHER, WILLIAM I

An engineering approach to digital design.

Includes bibliographies and index.

1.–Digital electronics. 2.–Logic design.
3.–Machine theory. I.–Title.
TK7868.D5F5 621.3815 78-27177
ISBN 0-13-277699-5

Printed in the United States of America
10 9 8 7 6 5 4 3 2 1

Editorial/production supervision
and interior design by *Virginia Huebner*
Page layout by *Gail Cocker*
Cover design by *Edsal Enterprises*
Manufacturing buyer: *Gordon Osbourne*

PRENTICE-HALL INTERNATIONAL, INC., *London*
PRENTICE-HALL OF AUSTRALIA PTY. LIMITED, *Sydney*
PRENTICE-HALL OF CANADA, LTD., *Toronto*
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WHITEHALL BOOKS LIMITED, *Wellington, New Zealand*

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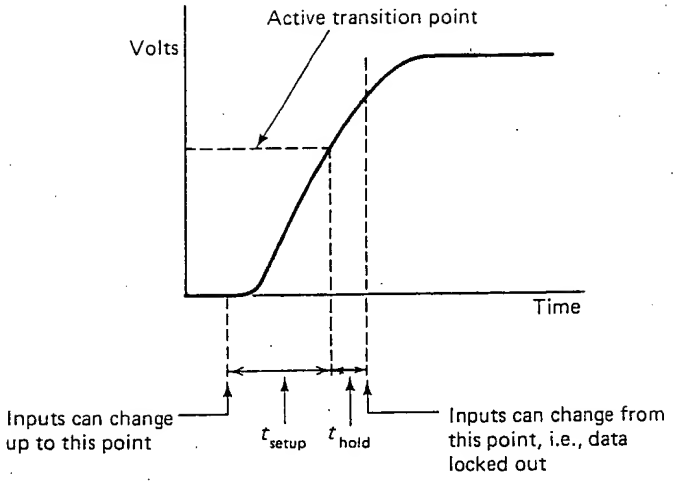
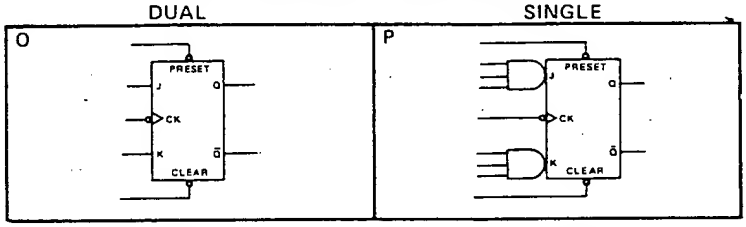


Fig. 5-37. A typical clock waveform for a rising-edge-triggered (RET) device expanded to illustrate the set-up time and the hold time definitions.

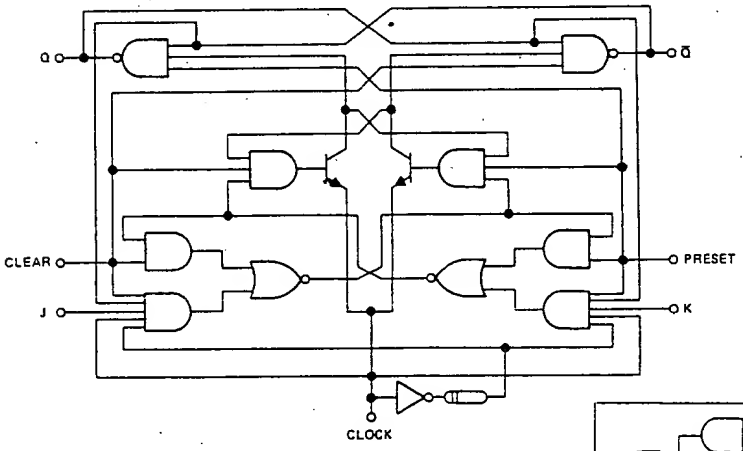
Fig. 5-38. Data sheets and logic diagrams for the SN74110 and SN74111. (Courtesy of Texas Instruments, Inc.)

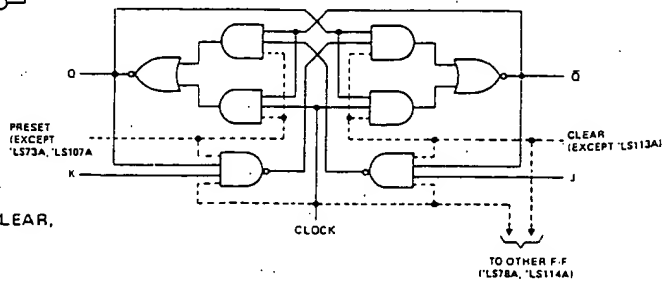
J-K FLIP-FLOPS WITH DATA LOCKOUT

	DUAL	SINGLE
	O	P



DWG. REF.	TYPICAL CHARACTERISTICS f_{max} (MHz)	Pwr/F-F (mW)	DATA TIMES SETUP (ns)	HOLD (ns)	DEVICE TYPE AND PACKAGE −55 C to 125 C		0 C to 70 C	
O	25	70	0†	30†	SN54111	J,W	SN74111	J,N
P	25	100	20†	5†	SN54110	J,W	SN74110	J,N





'LS73A, 'LS107A—DUAL J-K WITH CLEAR
'LS76A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET
'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113A—DUAL J-K WITH PRESET

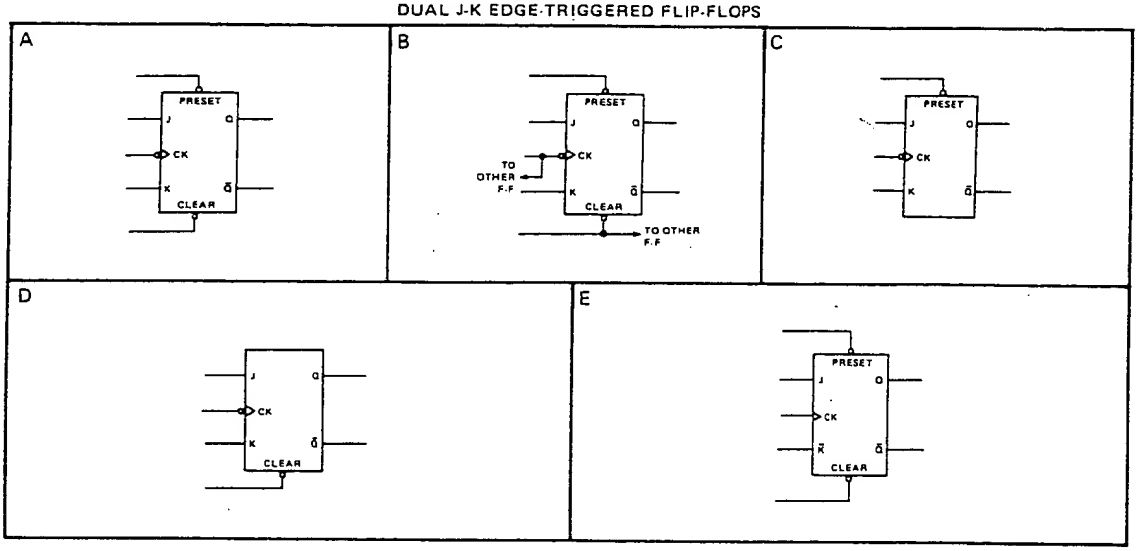
'LS73A, 'LS76A, 'LS78A, 'LS112A, 'LS113A, 'LS114A

† The arr

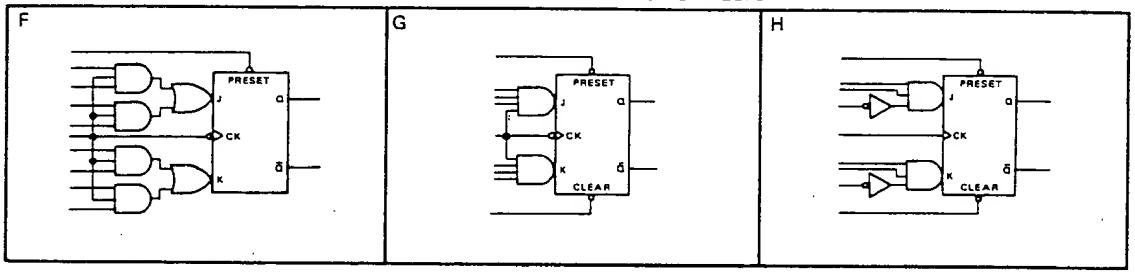
EXHIBIT A
page 4 of 6

waveform for a
evice expanded
d the hold time

DUAL J-K EDGE-TRIGGERED FLIP-FLOPS



SINGLE J-K EDGE-TRIGGERED FLIP-FLOPS



DWG REF.	TYPICAL CHARACTERISTICS		DATA TIMES		DEVICE TYPE AND PACKAGE				PAGE REFERENCES	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C		0°C to 70°C		PIN ASSIGNMENTS	ELECTRICAL
A	125	75	3↓	0↑	SN54S112	J, W	SN74S112	J, N	5-34	6-58
	50	100	13↑	0↑	SN54H106	J, W	SN74H106	J, N	5-32	6-52
	45	10	20↑	0↑	SN54LS76A	J, W	SN74LS76A	J, N	5-23	6-58
	45	10	20↑	0↑	SN54LS112A	J, W	SN74LS112A	J, N	5-34	6-56
B	125	75	3↓	0↑	SN54S114	J, W	SN74S114	J, N	5-34	6-58
	50	100	13↑	0↑	SN54H108	J, W	SN74H108	J, N	5-32	6-52
	45	10	20↑	0↑	SN54LS78A	J, W	SN74LS78A	J, N	5-24	6-56
	45	10	20↑	0↑	SN54LS114A	J, W	SN74LS114A	J, N	5-34	6-56
C	125	75	3↓	0↑	SN54S113	J, W	SN74S113	J, N	5-34	6-58
	45	10	20↑	0↑	SN54LS113A	J, W	SN74LS113A	J, N	5-34	6-56
D	50	100	13↑	0↑	SN54H103	J, W	SN74H103	J, N	5-31	6-52
	45	10	20↑	0↑	SN54LS73A	J, W	SN74LS73A	J, N	5-22	6-56
	45	10	20↑	0↑	SN54LS107A	J	SN74LS107A	J, N	5-32	6-56
E	33	10	20↑	5↑	SN54LS109A	J, W	SN74LS109A	J, N	5-33	6-56
	33	45	10↑	6↑	SN54109	J, W	SN74109	J, N	5-33	6-46
F	50	100	13↑	0↑	SN54H101	J, W	SN74H101	J, N	5-31	6-52
G	50	100	13↑	0↑	SN54H102	J, W	SN74H102	J, N	5-31	6-52
H	35	65	20↑	5↑	SN5470	J, W	SN7470	J, N	5-21	6-46

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

Fig. 5-39. Data sheet for RET and FET. JK Flip-Flops. (Courtesy of Texas Instruments, Inc.)

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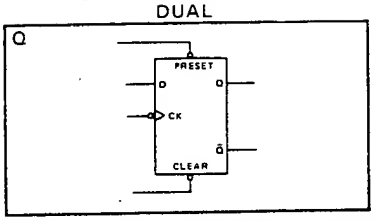
D-TYPE FLIP-FLOPS
DUAL



DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C	0°C to 70°C
Q	110	75	3↑	2↑	SN54S74	SN74S74
	43	75	15↑	5↑	SN54H74	SN74H74
	33	10	25↑	5↑	SN54LS74	SN74LS74
	25	43	20↑	5↑	SN5474	SN7474
	3	4	50↑	0↑	SN54L74	SN74L74

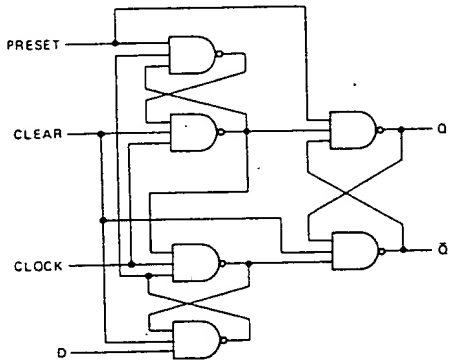


Fig. 5-40. Data and specification sheets for RET D Flip-Flops. (Courtesy of Texas Instruments, Inc.)

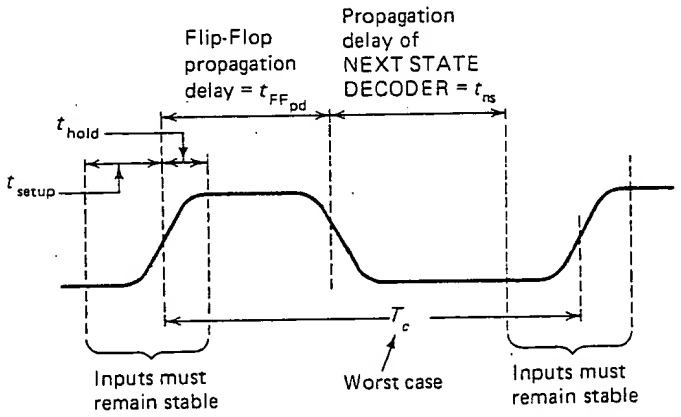


Fig. 5-41. Worst case timing related to maximum clock frequency determination.

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The logic diagrams for the devices shown in Figures 5-36, 5-37, 5-38, and 5-39 are vastly different from those developed earlier. The reason for this is twofold:

(1) These devices incorporate the edge-trigger or lock-out features.
(2) The actual integrated circuit manufacturing processes many times dictate a particular logic form.

However, the EXCITATION TABLES for these IC devices are identical to those we have developed. Also, note that the rising-edge of the clock for the SN74111 locks the data into the master cell and the falling-edge transfers this data to the outputs, providing advantages or disadvantages depending on the circumstances.

We see in Chapter 10 how Flip-Flops with edge-triggering and data lock-out features can be designed in a straightforward manner. However, we use these devices and other similar devices to our advantage in the next several chapters to implement a variety of finite-state machines.

5-20 TIMING AND TRIGGERING CONSIDERATIONS

It should be noted that two important timing constraints are listed in the typical data sheet listing shown in Figures 5-38, 5-39, and 5-40. These are SET-UP and HOLD times. The definition of *SET-UP time is the time required for the input data to settle in before the triggering edge of the clock.* If you choose to ignore this specification, you should expect unpredictable behavior. This unpredictable behavior manifests itself in several ways:

(1) missed data or ignored actions;
(2) possible partial transient outputs.

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These partial transient outputs are referred to as "partial SET" and "partial RESET" outputs. In other words, it is possible to start a RESET or SET operation, causing the output to start to change, but to fall back to its original state. Worse yet, a metastable condition can be precipitated in which the Flip-Flop is neither SET nor RESET for some undeterminable time. These concepts are fundamental in nature and are discussed at length in Chapter 7.

The definition of *HOLD time is the time required for the data to remain stable after the triggering edge of the clock.* Again, if you choose to ignore this specification, unpredictable behavior will result.

In keeping with this odd behavior constraint, these critical timing specifications also help determine the maximum allowable clock frequency for a finite-state machine. With all constraints included, Figure 5-41 illustrates how the worst case $t_{SET\text{-}UP}$, t_{HOLD}, Flip-Flop propagation delay and propagation delay of the NEXT STATE DECODER add together to determine the maximum clock frequency.